NEW SCHEME

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Fourth Semester B.E. Degree Examination, July/August 2005
BM/EC/EE/TE/ML/IT
Microprocessors

Time: 3 hrs.]   [Max.Marks : 100

Note: *1. Answer any FIVE full questions.*
2. All questions carry equal marks.

1. (a) Give a general block diagram of a microprocessor based system. Explain briefly the various blocks of the system. Give some examples of the types of devices used for each block.   **(10 Marks)**

(b) Give a list of the registers of 8085 that are accessible to the programmer. Explain what each of these registers are generally used for.   **(10 Marks)**

2. (a) Give two examples for each of the following types of instructions and indicate what each of these instructions do :

i)   Instructions with implied addressing

ii)   ALU type of instructions

iii) Instructions addressing memory indirectly through any register pair.

iv)   Conditional branch instructions.

v)   Interrupt related instructions.   **(10 Marks)**

(b) Consider the fetch and execute operations of the instruction "MOV M, A". Assume ready line is not activated, and answer the following :

i)   How many T-cycles and how many machine cycles would be required ?

ii)   What control signals are produced during each of the machine cycles ?

iii) In which T-cycles do the A/D pins carry the data ?

iv)   Which register produces the address during each of the machine cycles.

v)   What would be the status signals $S0$ & $S1$ during the first machine cycle ?   **(10 Marks)**

3. (a) Explain the functions of following pins of 8085 :

i) $IO/\overline{M}$

ii) S_0 and S_1

iii) HOLD/HLDA

iv)   READY   **(8 Marks)**

(b) Write an 8085 ALP to add two 16-bit data stored in consecutive memory locations and arrange to have the result stored in the following three memory locations, (using one byte location to store the carry, so that the result becomes a 24-bit value).   **(12 Marks)**

4. (a) Write an 8085 ALP subroutine to produce a delay of 1 second. Consider the 8085 clocked at 5 MHz. **(10 Marks)**

(b) Write an 8085 ALP subroutine to convert a 2-digit BCD number to a 2-digit hex number. **(10 Marks)**

5. (a) Design a circuit to interface a 4kB RAM using 6116 from address 8000H, and 4KB ROM using 2716 from address OOOOH. Assume demultiplexed address and data buses are available. Complete address decoding is required. **(10 Marks)**

(b) Explain :

     i) Memory mapped I/O

     ii) I/O mapped or standard I/O

     iii) Serial I/O

in connection with an 8085 processor system. Indicate the advantage of each of the above I/O types. **(10 Marks)**

6. (a) Consider an 8085 processor is enabled to accept interrupt through any of its interrupt accepting pins. How would you disable it selectively so as not to accept interrupt through the pin RST 6.5 ?

If now the processor is simultaneously interrupted through pins RST 5.5 and INTR, explain step-by-step how 8085 deals with the situation and services both the interrupts. **(10 Marks)**

(b) Interface an A/D converter to 8085 and write a program to convert the analog input to digital. **(10 Marks)**

7. (a) With circuit diagrams, explain how you would accomplish the following in an 8085 processor system.

     i) Interface a switch giving a single bit input to the processor (Use serial I/O pins)

     ii) Switch a 230 V power circuit on-or-off using a single bit from an 8-bit port interfaced to the processor. **(5+5 Marks)**

(b) Show how you would interface a keyboard to an 8085 processor using 8255. Write an ALP to generate a key code for the key pressed. **(10 Marks)**

8. (a) What is DMA operation ? Explain the features and operation of DMA controller 8257 with a block schematic. **(10 Marks)**

(b) With a block diagram, explain any ONE of the following chips :

     i) 8255 PPI

     ii) 8253 Timer **(10 Marks)**

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